Please amend the paragraph beginning on page 2, line 21 and ending on page 3, line 10, to read as follows:

Transistor elements 111, 112 have respective source regions 111b, 112b and respective drain regions 111c, 112c formed by introducing an impurity into semiconductor substrate 101 by way of ion implantation. The gaps between source regions 111b, 112b and drain regions 111c, 112c function as respective gate regions 111a, 112a. In cell array region 102, a pair of adjacent transistor elements 111 sharing source region 111b make up memory cell 110. A plurality of memory cells are arranged in a substantially zigzag pattern (see Fig. 2). In peripheral circuit region 103, transistor elements 112 are arranged as desired to form peripheral circuits, though not shown. As a whole, transistor elements 112 in peripheral circuit region 103 are arranged at a density lower than transistor elements 111 in cell array region 102.

IN THE ABSTRACT:

Please replace the existing Abstract of the Disclosure with an Abstract of the Disclosure provided at the end of this Amendment and Reply.

IN THE CLAIMS:

Please cancel claims 5, 10, 17 and 24 without prejudice or disclaimer.